Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1. (previously presented) In a multiprocessor digital signal processing system, the combination comprising;

a plurality of processors; and

a single coder/decoder having a digital/analog conversion channel time division multiplexed among, and an analog/digital conversion channel concurrently coupled to, said plurality of processors.

2. (previously presented) In a multiprocessor digital signal processing system according to claim 1, further comprising:

means for individually selecting input digital signals and analog signals for digital/analog conversion and analog/digital conversion, respectively; and

means for assigning which of said plurality of processors is coupled to said digital/analog conversion channel.

3. (previously presented) A digital signal processing system comprising:

a single coder/decoder having a digital signal input, an analog signal input, a digital/analog conversion channel, and an analog/digital conversion channel;

a first source of an analog input signals coupled to said analog signal input of said single coder/decoder;

a second source of digital input signals coupled to said digital signal input of said single coder/decoder;

a first plurality of processors multiplexed to said digital signal input of said coder/decoder; and

means for time division multiplexing said first plurality of processors to said digital signal input of said single coder/decoder;

whereby an analog-to-digital converted signals is concurrently accessible to all of said first plurality of processors.

4. (previously presented) The digital signal processing system according to claim 3, further comprising:

a second plurality of processors coupled to a digital output of said single coder/decoder for operating on said analog-to-digital converted signal.

5. (previously presented) The digital signal processing system according to claim 4, wherein each of said first plurality of processors comprise:

a register to buffer digital signal data for use by said digital signal input of said single coder/decoder.

6. (previously presented) The digital signal processing system according to claim 1, further comprising:

a plurality of registers to buffer digital signal data from said single coder/decoder to each of said first plurality of processors.

7. (previously presented) The digital signal processing system according to claim 6, further comprising:

means for individually selecting time slots for digital signals from each of said first plurality of processors to access said digital signal input of said coder/decoder.